

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the above-identified application:

Listing of Claims

Claims 1-37(Canceled).

Claim 38 (Currently Amended): A digital information coding apparatus, comprising:

- a) an input unit, arranged to selectively input first digital information data ~~that one sample is expressed with N bits~~ and second digital information data ~~that one sample is expressed with N bits~~, the first digital information data being different from the second digital information data;
- b) ~~as a first encoder~~, arranged to encode the first digital information data and output parallel data of L bits ~~to generate third digital information data that one sample is expressed with M bits ($M < N$);~~
- c) a second encoder, arranged to encode the second digital information data and output parallel data of M bits ($L \neq M$);
- d) a first converter, arranged to convert the parallel data of L bits generated by said first encoder, into first parallel data of N bits ($L \neq N$); ~~third digital information data generated by said encoder into fourth digital information data that plural samples are expressed with N bits, wherein said converter converts the third digital information data into the fourth digital information data by combining plural samples of the third digital information data; and~~
- e) a second converter, arranged to convert the parallel data of M bits generated by

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said second encoder into second parallel data of N bits ($M \neq N$):

d f) an error correction unit, arranged to selectively add an error correction check code to the first parallel data and the second parallel data, and digital information data and the fourth digital information data,

said error correction unit performing a common addition processing irrespectively of the first parallel data and the second parallel data digital information data and the fourth digital information data.

Claim 39 (Currently amended): An apparatus according to claim 38, wherein said first encoder encodes the first digital information data to be encoded by differential pulse code modulation.

Claim 40 (Previously presented): An apparatus according to claim 38, wherein the second digital information data is a television signal in which a video signal and an audio signal are time-division multiplexed.

Claim 41 (Previously presented): An apparatus according to claim 38, further comprising a recording unit, arranged to record the data processed by said error correction unit on a recording medium.

Claim 42 (Currently amended): An apparatus according to claim 38, wherein the second fourth digital information data being inputted in an amount less than the first digital information data during a predetermined period of time.

Claim 43 (Currently amended): A digital information coding method comprising the steps of:

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selectively inputting first digital information data and second digital information data,
the first digital information data being different from the second digital information data that
one sample is expressed with N bits and second digital information data that one sample is
expressed with N bits;

encoding the first digital information data to generate parallel data of L bits ~~third digital~~
~~information data that one sample is expressed with M bits ($M < N$);~~

encoding the second digital information data to generate parallel data of M bits ($L \neq M$);

converting the parallel data of L bits into first parallel data of N bits ($L \neq N$) ~~third digital~~
~~information data generated in said encoding step into fourth digital information data that plural~~
~~samples are expressed with N bits, wherein said converting step converts the third digital~~
~~information data into the fourth digital information data by combining plural samples of the~~
~~third digital information data; and~~

converting the parallel data of M bits into second parallel data of N bits ($M \neq N$);

selectively adding an error correction check code to the first parallel data and the second
parallel data, and digital information data and the fourth digital information data;

said error correction check code adding step performing a common addition processing
irrespective of the first parallel data and the second parallel ~~digital information data and the~~
~~fourth digital information data.~~